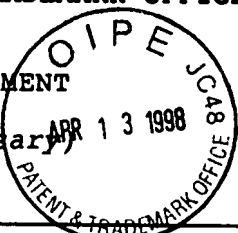


FORM PT01449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARI.006USF	SERIAL NO. 08/789,421
		APPLICANT Eliyahou Harari et al.	
		FILED January 29, 1997	GROUP 2511 2785

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)



U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LWH	A59	4 2 7 2 8 3 0	6/9/81	Moench	365	45	
LWH	A60	4 2 8 7 5 7 0	9/1/81	Stark	365	104	
LWH	A61	4 5 8 6 1 6 3	4/29/86	Koike	365	104	
LWH	A62	4 6 5 3 0 2 3	3/24/87	Suzuki et al.	365	104	
LWH	A63	4 8 4 7 8 0 8	7/11/89	Kobatake	365	104	
LWH	A64	4 8 9 9 2 7 4	2/6/90	Hansen et al.	395	200.52	
LWH	A65	4 9 5 8 3 1 5	9/18/90	Balch	375	500	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
LWH	B20	2 2 0 2 3 4 9	7/1988	UK Patent Appln.	—	—	yes
LWH	B21	3 8 1 2 1 4 7	5/1988	Deutschland	—	—	yes
LWH	B22	0 2 8 4 9 8 1	7/1988	European Patent Appln.	—	—	yes
LWH	B23	61 - 2 5 2 2 9	4/1986	Japanese Patent Appln.	—	—	yes

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

LWH	C11	Stark, M., "Two Bits Per Cell Rom," <u>IEEE Catalog No. 81-CH1626-1</u> , Library of Congress No. 80-85186, Order No. 341, Spring Comp Con 1981, Feb. 23-26, Twenty-Second Computer Society International Conference, San Francisco, CA
LWH	C12	Furuyama et al., "An Experimental 2-Bit/Cell Storage Dram For Macro Cell Or Memory-On-Logic Application," pp. 4.4.1 - 4.4.4, <u>IEEE</u> , (1988)
LWH	C13	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Levels Cell Storage," <u>IEEE Journal Of Solid-State Circuits</u> , Vol. 23, No. 1, February 1988
LWH	C14	Krick, P.J., "Three-State MNOS Fet Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, pps. 4192-4193 (May, 1976)
LWH	C15	Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 7A, pps. 3311-3314 (December 1981)
LWH	C16	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 3 (June, 1987)

EXAMINER <div style="font-size:2em; font-family: cursive;">Ly V. Hua</div>	DATE CONSIDERED Dec 13, 1998
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* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PT01449
(REV. 8-83)U.S. DEPARTMENT OF COMMERCE
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ATTY. DOCKET NO.

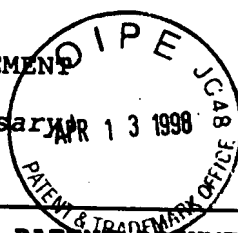
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APPLICANT

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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>LVH</i>	A66 4 7 2 7 5 1 2	2/23/88	Birkner et al.	395	500	
<i>LVH</i>	A67 4 7 9 7 5 4 3	1/10/89	Watanabe	235	492	
<i>LVH</i>	A68 4 7 9 8 9 4 1	1/17/89	Watanabe	235	380	
<i>LVH</i>	A69 4 8 2 9 1 6 9	5/9/89	Watanabe	235	492	
<i>LVH</i>	A70 4 8 3 1 2 4 5	5/16/89	Ogasawara	2200	492	
<i>LVH</i>	A71 4 8 5 3 5 2 2	8/1/89	Ogasawara	235	380	
<i>LVH</i>	A72 4 8 9 1 5 0 6	1/2/90	Yoshimatsu	235	492	
<i>LVH</i>	A73 5 3 5 9 7 2 6	10/25/94	Thomas	395	500	

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B24 2 1 7 2 1 2 6	10/1986	UK Patent Appln.			yes

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

EXAMINER

Ly V. Hua

DATE CONSIDERED

Dec 3, 1998

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